IN THE SPECIFICATION:

Please replace the paragraph starting on line 6, page 8 with the following paragraph:

The NTSC encoder 42 is provided therein with a buffer read circuit 42a. The buffer read circuit 42a reads out YUV data stored in the buffer ~~42~~ 26b at a clock rate of 1/4 times that upon writing. Furthermore, the read YUV data is encoded with an NTSC format. The encoded data is converted into an analog signal by a not-shown D/A converter and outputted to a monitor 44. As a result, through-images are displayed on the monitor 44.

A1

Please replace the paragraph starting on line 21, page 8 with the following paragraph:

If the operator selects a one-shot mode and then depresses the shutter button 54, the CPU 46 reduces to a low level a write signal to be supplied to the ~~end~~ AND circuit 42c shown in Figure 2, thereby applying gating to a write request. As a result, YUV data is suspended from being read out of the SDRAM 38. The signal processing circuit 22 remains outputting YUV data, and continues writing it to the SDRAM 38.

A2

Please replace the paragraph starting on line 14, page 9 with the following paragraph:

Referring to Figure 2, the CPU 46 inputs a high level gate signal to AND circuits 45c and 45d provided in the JPEG CODEC 45. Due to this, the write request generating circuit 45a and read request generating circuit 45b outputs in predetermined timing requests to be supplied to the mediation circuit 30a through the ~~ANC~~ AND circuits 45c and 45d. The mediation circuit 30a mediates between the requests and inputs a predetermined start signal to the processing circuit 30b.

A3

Please replace the paragraph starting on line 20, page 9 with the following paragraph:

During processing a write request, the processing circuit 30b reads shot image data from the SDRAM 38 and writes it to the buffer 26c through the bus 28. The shot image data written on the buffer 26c is read out by a buffer read circuit ~~45a~~ 45e provided in the JPEG CODEC 45, and then subjected to JPEG compression. The compressed image data is thereafter stored in a buffer 26d by a buffer write circuit ~~45b~~ 45f. The processing circuit 30b reads the compressed image data from the buffer 26b in response to a read request sent from the JPEG CODEC 45. The read compressed image data is again written to the SDRAM 38. This process is repeated with a result that compressed image data having been compressed of the shot image data is obtained within the SDRAM 38. Incidentally, each of the buffers 26c and 26d is also configured by a dual-port SRAM capable of storing 128-pixels of YUV data.

Please replace the paragraph starting on line 15, page 12 with the following paragraph:

Consequently, the CPU 46 in step S27 instructs the JPEG CODEC 45 to perform a compression process the ~~an~~ initial value Xb. The JPEG CODEC 45, in turn, requests the memory control circuit ~~20~~ 30 to read out shot image data B and performs a compression process on the shot image data B with the initial value Xb. The JPEG CODEC 45 also requests the memory control circuit 30 to write the compressed image data B. As a result, the compressed image data B is written to the SDRAM 38. The CPU 46 subsequently proceeds to step S29 to request the memory control circuit 30 to read out the compressed image data B, detect a size Yb of the read compressed data B, and calculates a next-time compression ratio Xl based on the size Yb, initial value Xb and target size Z. Specifically, Equation 1 is calculated. Thereafter, in step S30 the calculated compression ratio Xl is stored to the registers 46a and 46b.

A4

Please replace the paragraph starting on line 3, page 16 with the following paragraph:

Referring to Figure 7, the AE process will be explained in greater detail. The CPU 46 in step S251 first determines whether a vertical synchronizing signal has been inputted 5 or not. If "YES", in step S253 a luminance evaluation value is fetched, and in step S255 calculated is a shutter speed for an optimal exposure. Then, in step S257 the preceding shutter speed is subtracted from the calculated current shutter speed to determine a difference S between them. Thereafter, in

A5 cont

steps S259 and S263 the difference S is compared with a predetermined values a and -a. If S > a, then in step S261 the preceding shutter speed is added by the predetermined value a to obtain a value to be rendered as a current shutter speed. If ~~S < a~~ S < -a, in step S263 the predetermined value a is subtracted from the preceding shutter speed to obtain a value to be rendered as a current shutter speed. On the other hand, if "NO", in both the steps S259 and S263, the current shutter speed is not changed. Thereafter, in step S267 the current shutter speed is stored in the register 15a, and the process returns. In this manner, the shutter speed is brought to an optimal value at all times.